P27157.A04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : H. CHEN et al. Docket No. P27157

Appln. No. : 10/689,506 Confirmation No. 4303

Filed : October 20, 2003 Group Art Unit: 2813

Examiner: N. O. Berezny

For : HIGH PERFORMANCE STRESS-ENHANCED MOSFETs USING Si:C AND SiGe EPITAXIAL SOURCE/DRAIN AND METHOD OF MANUFACTURE

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria VA 22314

COVER LETTER TO SUBMIT EXECUTED RULE 1.131 DECLARATION

Sir:

The undersigned submits herewith three partially executed Rule 1.131 declarations that are executed by all of the inventors of the above-captioned application.

Applicants' representative forwarded a copy of the Rule 1.131 declaration along with Supplemental Request for Reconsideration Under 37 C.F.R. § 1.111 and Exhibit A to the inventors.

Inventor Dokumaci sent back four pages of the declaration by facsimile to Applicants' representative after signing and dating the declaration. Inventor Chen also sent back four pages of the declaration to Applicants' representative after signing and dating the declaration. Inventor Chidambarrao returned only the last page of the declaration to Applicants' representative after signing and dating the declaration.

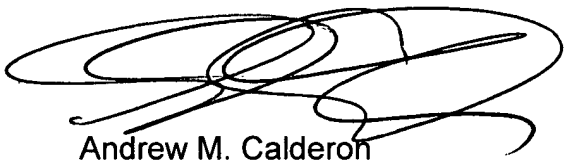
Applicants' representative has been advised by inventor Chidambarrao that all pages of the Rule 1.131 declaration were physically present when he signed and dated the

declaration.

Accordingly, Applicants respectfully submit herewith the three partially executed declarations as sent to Applicants' representative by the Inventors along with a copy of the Supplemental Request for Reconsideration Under 37 C.F.R. § 1.111 and Exhibit A added herein by Applicants' representative, and which are identical to those sent to the inventors along with the declaration.

Should there be any questions regarding this paper, please contact the undersigned at the below listed number.

Respectfully submitted,
H. CHEN et al.



Andrew M. Calderon
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November 24, 2005
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Haujie CHEN, *et al.*

Docket No. P27157

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DECLARATION UNDER 37 C.F.R. 1.131

Sir:

We, Huajie Chen, Dureseti Chidambarrao, and Omer H. Dokumaci do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1 and 10 of the above-identified application.

2. We completed the invention of claims 1 and 10 (and those claims dependent thereon) in the United States before June 17, 2003, as evidenced below.

CONCEPTION

3. Before June 17, 2003, we conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate, forming a pFET stack in the pFET channel and an nFET stack in the nFET channel, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice

constant of the substrate to create a compressive state within the pFET channel and providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel before June 17, 2003.

4. We also conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate, forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively, etching regions of the pFET structure and the nFET structure, forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel, forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel, and doping source and drain regions of the nFET and pFET structures.

5. Evidence of such conceptions as disclosed and recited in claims 1 and 10 of the application is shown in an embodiment of which is evidenced by IBM Invention Disclosure BUR8- 0318 (hereinafter referred to as "the Invention Disclosure") attached hereto as Exhibit A. The Invention Disclosure attached hereto is a photocopy of and are identical to the originals, except that all pertinent dates have been removed therefrom.

6. All relevant dates removed from the Invention Disclosure and other attached documents attached hereto are before June 17, 2003.

7. The benefits and features of the recited invention are shown and described in the Invention Disclosure and accompanying documents.

8. These features and others are exemplified in the figures accompanying the Invention Disclosure.

DUE DILIGENCE

9. At least inventor Dureseti Chidambarrao communicated with outside patent counsel, Andrew M. Calderon, in preparing a patent application based on the Invention Disclosure.

10. We worked diligently on the preparation of the patent application by first submitting the Invention Disclosure statement to in-house IBM counsel on June 9, 2003.

11. After a prior art search was conducted and the Invention Disclosure was mailed to outside counsel, Andrew M. Calderon, we worked diligently on the preparation of the patent application with outside patent counsel Andrew M. Calderon until a final

draft patent application was completed to our satisfaction. Communications took place between at least one of the Inventors and Mr. Calderon on at least August 26, 2003, September 20, 2003 and October 13, 2003.

12. A final draft of the patent application was forwarded to inventor Dureseti Chidambarrao on October 13, 2003 for execution of the formal documents by all of the inventors. The inventors signed the documents for filing in the U.S. Patent and Trademark Office, which was effectuated on October 20, 2003 by outside counsel.

13. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Huajie Chen — 10/26/05
Huajie Chen — Date

Dureseti Chidambarrao — Date

Omer H. Dokumaci — Date

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Huajie Chen	Date
Dureseti Chidambarrao	11/17/05 Date
Omer H. Dokumaci	Date

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Haujie CHEN, *et al.*

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constant of the substrate to create a compressive state within the pFET channel and providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel before June 17, 2003.

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Huajie Chen	Date
Dureseti Chidambarrao	Date
Omer H. Dokumaci	11/16/05 Date

Disclosure FIS8- -0318

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By DURESETI CHIDAMBARRAO On
Last Modified By DURESETI CHIDAMBARRAO On

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (in English)**

High Performance Stress-Enhanced MOSFETs Using Si:C and SiGe epi Source/Drain: Method & Structure

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(DKL) DKL ... ABERNATHEY: 256MB DRAM "Non-Alliance" Only
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Submitted Date		
*Owning Division	select	TG
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: DURESETI CHIDAMBARRAO/Fishkill/IBM, Omer Dokumaci/Fishkill/IBM, Huajie Chen/Fishkill/IBM

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Chen, Huajie	1A2061	29/7K3A	532-9633	Schepis, Dominic

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Inventors without a Blue Pages entry

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Response Due to IP&L	

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Stresses are known to affect device drive currents. Tensile longitudinal stress along the channel is known to help the nFET drive currents while it degrades the pFET. There have been many proposals to improve both nFET and pFET device performance using tensile and compressive longitudinal stresses, respectively, which include modulating spacer intrinsic stresses and STI material changes individually for the two MOSFETs using masks. Here we show a way to bring longitudinal tensile stress very close to the nFET channel while at the same time bringing compressive stress in the pFET.

For the pFET we had proposed in a previous disclosure (FIS8-2003-0116) SiGe embedded source/drain regions to stress the pFET channel compressively. In the invention described here, for the nFETs we propose using Si:C. In addition we also provide a process and structure to integrate both SiGe and Si:C materials into CMOS technology. This highly tensile Si:C film is embedded in the silicon substrate in the source/drain regions to longitudinally apply tension on the nFET in the channel just under the gate. The key here is to use the Si:C only in the nFET S/D regions. This invention also integrates SiGe in the S/D regions of the pFET, as previously disclosed.

Before Si:C can be proposed as a material of choice, there needs to be some demonstrated proof of feasibility particularly since it's application into standard CMOS is quite new. There are questions of integration into standard processing and the relevance of its material properties. Here we discuss background information regarding Si:C which shows that it has the correct stress, that it can include the correct amount of C content, and that it can be grown epitaxially and selectively.

Background Information on Si:C

Si:C is known to grow epitaxially on Si where it is inherently tensile. A 1% C content in a Si:C/Si material stack can cause tensile stress levels in the Si:C on the order of 500MPa. In comparison, in the SiGe/Si system about 6% Ge is needed to causes a 500MPa compression. This 1% level of C can be readily incorporated into Si during epitaxial growth as shown in Ernst et al, VLSI Symp., 2002, p92.

In Ernst et al, they make use of Si/Si:C/Si layered channels for nFETs. However, their structure is very different from ours. They use the Si:C in the more traditional strained Si approach as a stack of layers in the channel, but they do not strain the silicon cap through relaxing the Si:C. Instead they are using the Si:C as part of the channel itself. The problem with this approach is that the mobility was not enhanced, but retarded depending on the C content from scattering. In this invention we do not use the Si:C as a directly built up stacked layer under the channel (as in the paper and for example in strained Si on SiGe

applications) but as a replacement material for nFET S/D regions that are in tension and therefore imposing tension in the channel region also. This Si:C therefore applies to nFETs while the pFETs are implemented with SiGe.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

The main conceptual point of this invention is to grow Si:C epi layer only in the source and drain region of the nFET transistor while growing SiGe in the pFET region. Just like the SIGe layer, the Si:C layer is relatively thin (below its critical thickness) and is not relaxed. The transistor channel region of the nFET is strained by the stress from the Si:C epi layer (similar to the compressive stress from the SiGe in the pFET). Since the Si:C layer is embedded in the source/drain region, low resistance silicide can still be formed. Interestingly, embedded (sub-surface or coplanar-to- surface) Si:C films can put larger stresses than the above-surface Si:C counterparts because of the film surface not being free. In this invention the different heights and protrusions of the Si:C whether embedded or coplanar with the surface or raised are being covered.

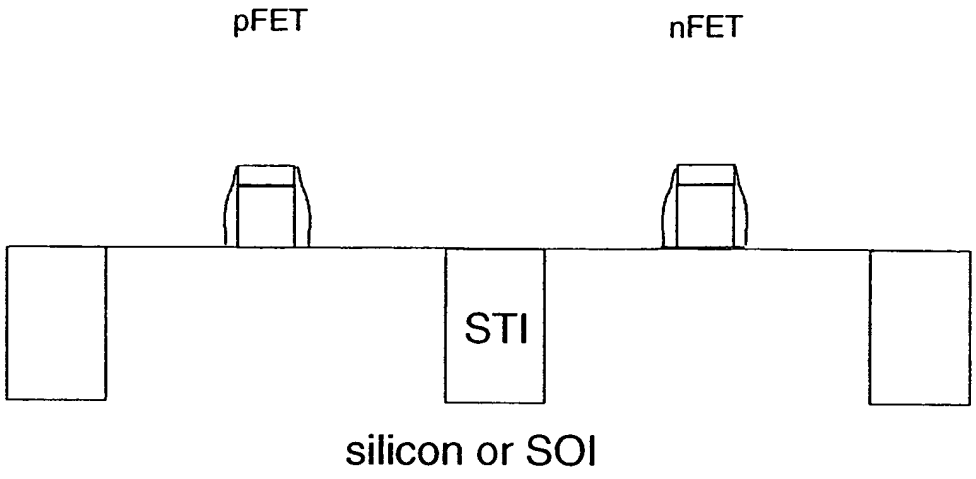
Advantages

In other strained Si approaches for applying tension on the nFET, SiGe is used as part of the whole substrate. When Si is grown epitaxially on the relaxed SiGe layer, a tensile strain is resulted in in the Si, which improves electron mobility. However, the technique requires SiGe to be relaxed, which demands a very thick SiGe layer (i.e., 0.5-1micron). As the SiGe relaxes, a dense network of dislocations form causing yield issues. Further, the cost of the process is also quite prohibitive. Some techniques such as graded Ge concentration and CMP are used to improve the quality of the films, but in general, this process is plagued by high density of defects and costs. In our approach we do not have to deposit thick films. Typically we expect to deposit Si:C and SiGe films that are 10-100nm thick. This provides a more cost-effective way to add stress to the MOSFETs.

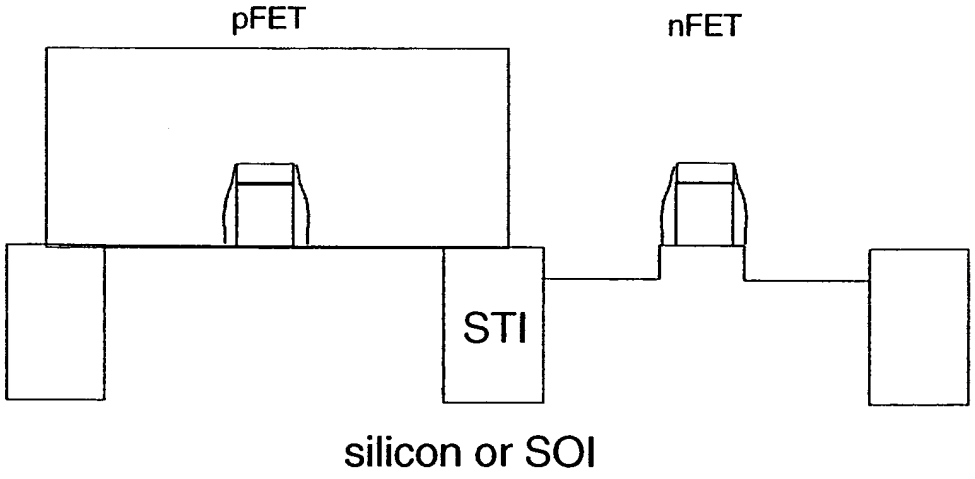
3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

Embodiment 1

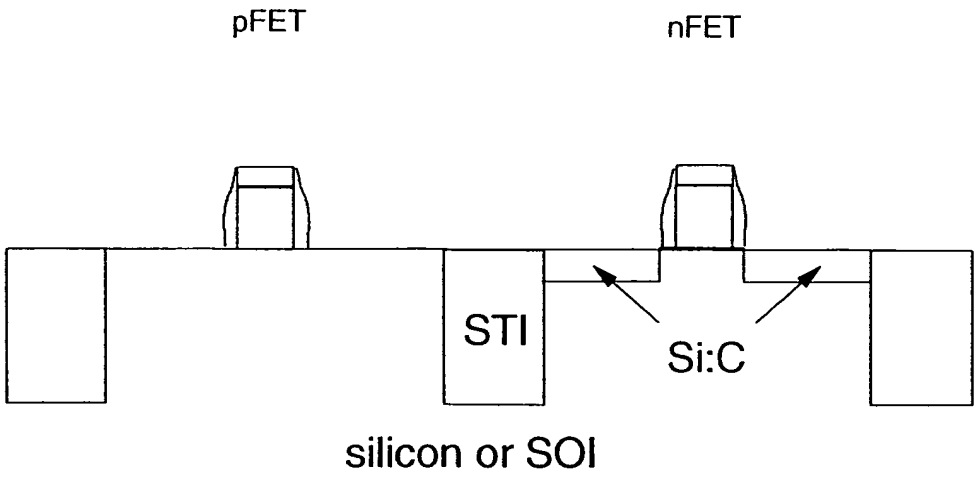
Step 1: For bulk or SOI substrates build STI, gate stacks for nFETs and pFETs, spacers, and TEOS cap on gates



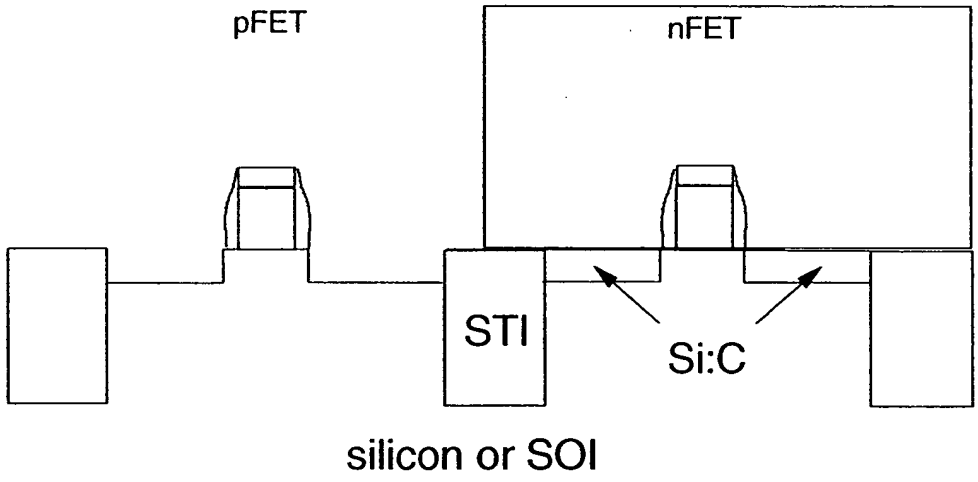
Step 2: Deposit thin liner, Mask pFET and etch nFET S/D regions



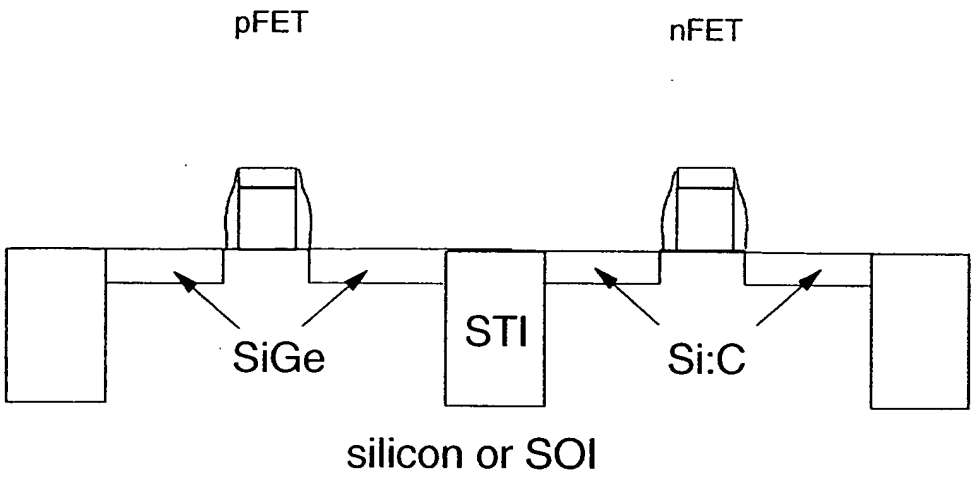
Step 3: Grow "highly tensile" selective Si:C epi in nFET S/D regions and remove resist



Step 4: Deposit thin liner, Mask nFET and etch pFET S/D regions



Step 5: Grow "highly compressive" selective SiGe epi in pFET S/D regions, remove resist, and remaining liner



Step 6: Continue MOSFET processing

(a) RSD Si epi that facilitates CoSi processing or NiSi processes that are known to work on SiGe & Si:C

(b) .... Further standard CMOS processing after this

Embodiment 2

In this embodiment we cover the issues of the thickness of both the selective SiGe and Si:C. They can be buried (or embedded), co-planar with the silicon surface, or protrude above the Si surface depending on the process. For stress reasons, there should be some embedded structure.